REMARKS/ARGUMENTS

Favorable reconsideration of this application, in light of the following discussion, is respectfully requested.

Claims 1-20 are pending; and no claims are amended, newly added, or canceled herewith.

In the outstanding Office Action, the abstract was objected to as including informalities; Claims 1-3 and 7-9 were rejected under 35 U.S.C. §103(a) as unpatentable over Sachdev (U.S. Pat. No. 6,134,688) in view of Whetsel (U.S. Pat. No. 6,189,115); Claims 5, 6, 11-16, 19 and 20 were rejected under 35 U.S.C. 103(a) as unpatentable over Sachdev and Whetsel in view of Applicant's Admitted Prior Art (herein "AAPA"); and Claims 4, 10, 17 and 18 were objected to as dependent upon a rejected based claim but would be allowable in independent form.

Initially, Applicants gratefully acknowledge the early indication of the allowable subject matter in Claims 4, 10, 17 and 18. However, since Applicants consider that Claims 1 and 13 patentably define over the cited art, Claims 4, 10, 17 and 18 have presently been maintained in dependent form.

Before turning to the outstanding prior art rejections, it is believed that a brief review of the present invention would be helpful.

In this regard, the claimed invention describes a scan test circuit. In a non-limiting example the claimed invention will be described in relation to the prior art.

In the prior art, a scan test was performed only to test the switching function of the logic circuit connected between the flip-flop circuits and could not test whether the flip-flop circuit of the following stage could receive a change of data with the delay time at its actual operation speed. The conventional scan test had timings of scan shift and capture, as shown in Fig. 2.

A predetermined data was set in the preceding flip-flop circuit at the scan shift timing, and the result of the logic operation between the preceding flip-flop circuit and the following flip-flop circuit was obtained at the capture timing. The time interval between the scan shift timing and the capture timing, e.g. 30 as in Fig. 6, depended on the performance of the tester.

Therefore, the performance of the tester needed to be improved, that is, the scan clock frequency needed to be higher when the time interval between the scan shift timing and the capture timing needed to be shortened in order to implement an at-speed scan test. Further, it was also necessary to set the shift data from the shift data input/output port I/O at a high speed in order to implement the at-speed scan test.

However, testers used in the scan test to set the shift data that have an operation clock frequency that is as high as the clock frequency in the actual operation speed of semiconductor integrated circuits to be tested are very expensive. This is the conventional problem to be solved by the claimed invention.

In a non-limiting example the claimed invention describes that a scan test with consideration of desired timing can be achieved by controlling the change timing of an external select signal.

To achieve the above-mentioned function, the scan test circuit comprises a non-inversion/inversion control circuit inserted and connected between a sequential circuit and a combinational circuit included in a path to be subjected to a scan test, the non-inversion/inversion control circuit determining whether or not to invert the scan data output from the sequential circuit, on the outside of the sequential circuit using an arbitrary timing.

Furthermore, the scan test circuit includes a first sequential circuit, with shift data corresponding to output data to be observed being set in the first sequential circuit by a scan shift conducted one repetition period before capture of the output data and scan data corresponding to the shift data being output by the first sequential circuit, a non-

inversion/inversion control circuit, which does not invert or in contrast inverts the scan data output from the first sequential circuit, on the outside of the first sequential circuit at an arbitrary timing, a combinational circuit included in a path to be subjected to scan test, and supplied with scan data obtained by non-inverting or inverting the scan data by means of the non-inversion/inversion control circuit and a second sequential circuit to capture output data output from the combinational circuit according to the scan data.

Therefore, the claimed invention excludes the influence of the performance of the tester, i.e., the scan clock frequency, and the shift data set speed from the shift data input/output port I/O depending on the LSI by introducing the timing controlled external select signal. As a result, the at-speed scan test can be executed simply and at a low cost.

Turning now to the §103(a) rejections over Sachdev and Whetsel, Applicants respectfully traverse these rejections.

Claim 1, recites,

> A scan test circuit comprising a noninversion/inversion control circuit inserted and connected between a sequential circuit and a combinational circuit included in a path to be subjected to a scan test, said noninversion/inversion control circuit not inverting or inverting scan data output from said sequential circuit, on outside of said sequential circuit at arbitrary timing.

Claim 13 recites similar features.

Sachdev discloses an electronic device, with a plurality of logic stages for functional collaboration, that is provided with selection means for selectively operating the plurality of logic stages to form either a sequential logic circuit or a combinatorial logic circuit.

Specifically in Figs. 2 and 4 and col. 6, lines 10-30, Sachdev discloses device 400 having a selection means 402 for reversibly and functionally converting the sequential logic circuit into a combinatorial logic circuit.

However, Sachdev does not disclose or suggest that the non-inversion/inversion control circuit not inverting or inverting scan data output from said sequential circuit, on outside of said sequential circuit at arbitrary timing, as recited in Claim 1.

In other words Sachdev does not describe controlling the change timing of the internal data in the logic circuit by the external select signal. In contrast, Sachdev merely discloses how to select logic stages to be combined to form either a sequential logic circuit or a combinatorial logic circuit.

The outstanding Office Action relies on Whetsel as curing the above noted deficiencies in Sachdev.

Whetsel discloses the combinational circuit included in a path to be subjected to a scan test as shown in Fig. 7. Further, Whetsel describes that a test bus controller is included in the path of the combinational circuit and the test bus controller inputs the test mode select (TMS) and the test clock (TCK) to each of ICs 1-N, IC (T), and IC 1-M simultaneously.

In contrast Claim 1 recites a noninversion/inversion control circuit not inverting or inverting scan data output from said sequential circuit, on outside of said sequential circuit at arbitrary timing.

In other words, Whetsel describes that the test bus controller is included in the path of the combinational circuit, but is not an outside component of the combinational circuit. Further, Whetsel describes that the test bus controller input the test mode select (TMS) and the test clock (TCK) to each of ICs 1-N, IC (T), and IC 1-M simultaneously, but not at arbitrary timing.

Further, AAPA does not cure the above noted deficiencies of Sachdev and Whetsel.

Accordingly, Applicants respectfully submit that Claims 1 and 13 and claims depending therefrom patentably distinguish over Sachdev, Whetsel, and AAPA considered individually or in any proper combination.

Consequently, no further issues are believed to be outstanding in the present application, and the present application is believed to be in condition for formal Allowance. A Notice of Allowance for Claims 1-20 is earnestly solicited.

Respectfully submitted,

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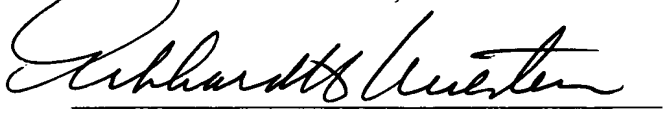

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